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EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,253	JEDDELOH ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-50 are presented for examination. This office action is in response to the amendment filed on 12/12/05.

2. The information disclosure statement (IDS) submitted on 12/12/05 is being considered by the examiner.

3. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies

subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

4. Applicants are requested to update the status of the related U.S. patent application, accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.). Also applicants are requested to include the status of the related U.S. applications or patents CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification, if any.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6,13, 40-44, and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by Mote et al. (Mote) U.S. Patent No. 5,638,534.

As to claim 1, Mote discloses the invention as claimed. Mote discloses a memory module, comprising: a plurality of memory devices (Fig. 1 Refs. 135); and a memory hub (Fig. 1 Ref. 130), comprising: a link interface receiving memory requests for access to at least one of the memory devices (Fig. 1 Ref. 130 and col. 2 lines 34-41); a memory device interface (Fig. 1 Ref. 130 to Ref. 135) coupled to the memory devices, the memory device interface being operable to transmit memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests (col. 2 lines 34-41); a posted write buffer (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit the write memory requests to the memory device interface (col. 1 lines 50- 59); and a read request path operable to transmit read memory requests from the link interface to the

memory device interface and to transmit read data from the memory device interface to the link interface (Fig. 1 Ref. 130 to Ref. 135 and col. 2 lines 34-41).

As to claim 2, Mote further discloses wherein the read request (col. 1 line 60 thru col. 2 line 8 & col. 9) path comprises a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to transmit memory requests to the memory device interface responsive to memory requests received from the link interface.

As to claim 3, Mote further discloses wherein the posted write buffer comprises coherency circuitry (col. 1 line 60 thru col. 2 line 8 & col. 10 lines 34-51 and comparison and pointer logic) that is operable to receive read memory requests from the link interface and is operable to determine if read data called for by the read request is stored in the posted write buffer and to generate a hit signal (Fig. 8 Ref. 230 and col. 10 lines 34-51, comparison and pointer logic reads on this limitation) responsive thereto, and wherein the memory sequencer is coupled to receive the hit signal from the posted write buffer and is operable to transmit memory requests to the memory device interface responsive to memory requests received from the link interface only in the absence of the hit signal (Fig. 8 Ref. 230 and col. 10 lines 34-51, comparison and pointer logic reads on this limitation).

As to claim 4, Mote further discloses wherein the posted write buffer (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) is operable to transmit the write memory requests to the memory device interface only when neither the memory hub nor the memory devices are busy servicing read memory requests.

As to claim 5, Mote further discloses wherein the posted write buffer further comprises coherency circuitry (col. 1 line 60 thru col. 2 line 8 & col. 10 lines 34-51 and comparison and pointer logic) coupled to receive read memory requests from the link interface, the coherency circuitry being operable to determine from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, the coherency circuitry being operable to transmit the read data responsive to the read memory request from the posted write buffer to the link interface in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface (col. 9 and col. 10 lines 34-51).

As to claim 6, Mote further discloses wherein the memory hub further comprises a multiplexer (col. 1 line 60 thru col. 2 line 8, data from posted write or DRAM reads on this limitation) having a first input port coupled to receive read data from the posted write buffer, a second input port coupled to receive read data from the memory device

interface and an output port (Fig. 1 Ref. 192 D0-D31) coupled to the link interface to apply read data to the link interface, the multiplexer further having a control terminal (Fig. 8 outputs from Refs. 230 and 206 or Fig. 7 Ref. 186) coupled to the posted write buffer, the posted write buffer generating a control signal to cause the multiplexer to couple the output port to the first input port in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, and to generate a control signal (Fig. 8 outputs from Refs. 230 and 206 or Fig. 7 Ref. 186) to cause the multiplexer to couple the output port to the second input port in the event the read memory request is not directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

As to claim 13, Mote further discloses wherein the memory devices comprise dynamic random access memory devices (Fig. 1 Ref. 135).

As to claim 40, Mote discloses the invention as claimed. Mote discloses a method of reading data from a plurality of memory modules (Fig. 1 Refs. 135), comprising: receiving memory requests (Fig. 1 Ref. 130 and col. 2 lines 34-41) at each of the plurality of memory modules, the memory requests requesting access to a memory device in the memory module, the memory requests including read requests and write requests (Fig. 1 Ref. 130 and col. 2 lines 34-41); coupling at least some of

the read memory requests to the memory device in the memory module receiving the read request; coupling read data from the memory module responsive to the read memory request; accumulating the write requests (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) in the memory module without immediately coupling the write requests to the memory devices in the memory module receiving the write request; and subsequently coupling each of the accumulated write requests to the memory device in the memory module receiving the write request (col. 1 line 60 thru col. 2 line 8 & col. 9 and col. 2 lines 34-41).

As to claim 41, Mote further discloses determining in each memory module receiving a read request if the read request is directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device; if the read request is directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device, coupling the read data from the accumulated write requests; and if the read request is not directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device, coupling the read data from the memory device (col. 1 line 60 thru col. 2 line 8 & col. 9).

As to claim 42, Mote further discloses determining in each memory module receiving a read request if the read request is directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device;

and if the read request is not directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device, coupling the read request to the memory device in the memory module receiving the read request (col. 1 line 60 thru col. 2 line 8 & col. 9).

As to claim 43, Mote further discloses wherein the act of subsequently coupling each of the accumulated write requests to the memory device in the memory module receiving the write request comprises subsequently coupling each of the accumulated write requests to the memory device in the memory module receiving the write request only when the memory device is not busy servicing a read request (col. 1 line 60 thru col. 2 line 8 & col. 9).

As to claim 44, Mote further discloses determining from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been accumulated but not yet coupled to the memory device; coupling the read data responsive to the read memory request from the accumulated write requests in the event the read memory request is directed to a memory address to which a write memory request has been accumulated but not yet coupled to the memory device (col. 1 line 60 thru col. 2 line 8 & col. 9).

As to claim 50, Mote further discloses wherein the memory devices comprise dynamic random access memory devices.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote et al. (Mote) U.S. Patent No. 5,638,534 in view of Sharma U.S. Patent Application Pub No. 2004/0019728.

As to claim 14, Mote discloses the invention as claimed. Mote discloses a memory hub (Fig. 1 Ref. 130), comprising: a link interface receiving memory requests (Fig. 1 Ref. 130 and col. 2 lines 34-41); a memory device interface (Fig. 1 Ref. 130 to Ref. 135) operable to output memory requests and to receive read data responsive to the memory requests output by the memory device interface; a posted write buffer (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit the write memory requests to the memory device interface(col. 1 lines 50- 59); and a read request path operable to transmit read memory requests from the link interface to the memory device interface and to transmit read data from the memory device interface to the link interface(Fig. 1

Ref. 130 to Ref. 135 and col. 2 lines 34-41), however, Mote does not specifically disclose the link interface receiving memory requests from a memory controller.

Sharma discloses a link interface receiving memory requests from a memory controller (Fig. 1 North Bridge) for the purpose of integrate multiple functions in one chip thereby reduce space, delay and easy of use by the end users.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the link interface receiving memory requests from a memory controller as taught by Sharma into the system of Mote for the advantages stated above.

As to claim 15, Mote further discloses wherein the read request (col. 1 line 60 thru col. 2 line 8 & col. 9) path comprises a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to transmit memory requests to the memory device interface responsive to memory requests received from the link interface.

As to claim 16, Mote further discloses wherein the posted write buffer comprises coherency circuitry (col. 1 line 60 thru col. 2 line 8 & col. 10 lines 34-51 and comparison and pointer logic) that is operable to receive read memory requests from the link interface and is operable to determine if read data called for by the read request is stored in the posted write buffer and to generate a hit signal (Fig. 8 Ref. 230 and col. 10 lines 34-51, comparison and pointer logic reads on this limitation)

responsive thereto, and wherein the memory sequencer is coupled to receive the hit signal from the posted write buffer and is operable to transmit memory requests to the memory device interface responsive to memory requests received from the link interface only in the absence of the hit signal (Fig. 8 Ref. 230 and col. 10 lines 34-51, comparison and pointer logic reads on this limitation).

As to claim 17, Mote further discloses wherein the posted write buffer (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) is operable to transmit the write memory requests to the memory device interface only when neither the memory hub nor the memory devices are busy servicing read memory requests.

As to claim 18, Mote further discloses wherein the posted write buffer further comprises coherency circuitry (col. 1 line 60 thru col. 2 line 8 & col. 10 lines 34-51 and comparison and pointer logic) coupled to receive read memory requests from the link interface, the coherency circuitry being operable to determine from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, the coherency circuitry being operable to transmit the read data responsive to the read memory request from the posted write buffer to the link interface in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write

buffer and has not yet been coupled to the memory device interface (col. 9 and col. 10 lines 34-51).

As to claim 19, Mote further discloses wherein the memory hub further comprises a multiplexer (col. 1 line 60 thru col. 2 line 8, data from posted write or DRAM reads on this limitation) having a first input port coupled to receive read data from the posted write buffer, a second input port coupled to receive read data from the memory device interface and an output port (Fig. 1 Ref. 192 D0-D31) coupled to the link interface to apply read data to the link interface, the multiplexer further having a control terminal (Fig. 8 outputs from Refs. 230 and 206 or Fig. 7 Ref. 186) coupled to the posted write buffer, the posted write buffer generating a control signal to cause the multiplexer to couple the output port to the first input port in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, and to generate a control signal (Fig. 8 outputs from Refs. 230 and 206 or Fig. 7 Ref. 186) to cause the multiplexer to couple the output port to the second input port in the event the read memory request is not directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

7. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote et al. (Mote) U.S. Patent No. 5,638,534 in view of Sharma U.S. Patent Application

Pub No. 2004/0019728 and further in view of Shipp et al. (Shipp) U.S. Patent No. 5,796,413.

As to claim 20, Mote further discloses wherein the posted write buffer is operable to store posted write memory requests (Fig. 7 Ref. 184 and Col. 9. lines 1-27 and col. 1 lines 50-59). However, neither Mote nor Sharma specifically discloses the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit the posted write memory requests to the memory device interface.

Shipp discloses the number of posted write memory requests accumulated exceeds a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65), and to thereafter transmit the posted write memory requests to the memory device interface for the purpose of preventing data overflow and underflow (col. 7 line 1).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit the posted write memory requests to the memory device interface as taught by Shipp into the combined invention of Mote and Sharma for the advantages stated above.

As to claim 21, Mote, Sharma, and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to vary the predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) as a function of an operating parameter of the memory module.

As to claim 22, Mote, Sharma, and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to store posted write memory requests (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) until the posted write memory requests have been stored for more than a predetermined duration, and to thereafter transmit the posted write memory requests to the memory device interface.

As to claim 23, Mote, Sharma, and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to vary the predetermined duration (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) as a function of an operating parameter of the memory module.

As to claim 24, Mote, Sharma, and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to store posted write memory requests as long as the number of posted write memory requests accumulated does not exceed a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) and the posted write memory requests have not been stored for more than a predetermined duration (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65), and to transmit the posted write memory requests to the memory device interface if either the number of posted write memory requests accumulated exceeds the predetermined number or the posted write memory requests have been stored for more than the predetermined duration.

8. Claims 7-11 and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote et al. (Mote) U.S. Patent No. 5,638,534 in view of Shipp et al. (Shipp) U.S. Patent No. 5,796,413.

As to claim 7, Mote further discloses wherein the posted write buffer is operable to store posted write memory requests (Fig. 7 Ref. 184 and Col. 9. lines 1-27 and col. 1 lines 50-59). However, Mote does not specifically disclose the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit the posted write memory requests to the memory device interface.

Shipp discloses the number of posted write memory requests accumulated exceeds a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65), and to thereafter transmit the posted write memory requests to the memory device interface for the purpose of preventing data overflow and underflow (col. 7 line 1).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit the posted write memory requests to the memory device interface as taught by Shipp into the system of Mote for the advantages stated above.

As to claim 8, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to vary the predetermined

number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) as a function of an operating parameter of the memory module.

As to claim 9, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to store posted write memory requests (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) until the posted write memory requests have been stored for more than a predetermined duration, and to thereafter transmit the posted write memory requests to the memory device interface.

As to claim 10, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to vary the predetermined duration (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) as a function of an operating parameter of the memory module.

As to claim 11, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to store posted write memory requests as long as the number of posted write memory requests accumulated does not exceed a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) and the posted write memory requests have not been stored for more than a predetermined duration (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65), and to transmit the posted write memory requests to the memory device

interface if either the number of posted write memory requests accumulated exceeds the predetermined number or the posted write memory requests have been stored for more than the predetermined duration.

As to claim 45, Mote and Shipp disclose the invention as claimed above. Ship further discloses wherein the act of subsequently coupling each of the accumulated write requests to the memory device in the memory module receiving the write request comprises: accumulating write requests until the number of write requests accumulated exceeds a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65); and when the number of write requests accumulated exceeds the predetermined number, coupling the write requests to the memory device.

As to claim 46, Mote and Shipp disclose the invention as claimed above. Ship further discloses comprising varying the predetermined number as a function of an operating parameter of the computer system (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65).

As to claim 47, Mote and Shipp disclose the invention as claimed above. Ship further discloses wherein the act of subsequently coupling each of the accumulated write requests to the memory device in the memory module receiving the write request comprises: accumulating write requests until the write requests have been accumulated for more than a predetermined duration; when each of the write requests

has been accumulated for more than the predetermined duration, coupling the write request to the memory device (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65).

As to claim 48, Mote and Shipp disclose the invention as claimed above. Ship further discloses comprising varying the predetermined duration as a function of an operating parameter of the computer system (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65).

As to claim 49, Mote and Shipp disclose the invention as claimed above. Ship further discloses wherein the act of subsequently coupling each of the accumulated write requests to the memory device in the memory module receiving the write request comprises: accumulating write requests until the number of write requests accumulated exceeds a predetermined number or the write requests have been accumulated for more than a predetermined duration; and when the number of write requests accumulated exceeds the predetermined number or when a write request has been accumulated for more than the predetermined duration, coupling the write request to the memory device (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mote et al. (Mote) U.S. Patent No. 5,638,534 in view of Sanchez-Olea U.S. Patent Pub 2002/0178319.

As to claim 12, Mote discloses the invention as claimed above. However, Mote does not specifically disclose the link interface comprises an optical input/output port.

Sanchez-Olea discloses the link interface comprises an optical input/output port (Fig. 1 Ref. 1106) for the purpose of providing a newer and faster interface.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the link interface comprises an optical input/output port as taught by Sanchez-Olea into the system of Mote for the advantages stated above.

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mote et al. (Mote) U.S. Patent No. 5,638,534 in view of Sharma U.S. Patent Application Pub No. 2004/0019728 and further in view of Sanchez-Olea U.S. Patent Pub 2002/0178319.

As to claim 25, Mote and Sharma disclose the invention as claimed above. However, neither Mote nor Sharma specifically discloses the link interface comprises an optical input/output port.

Sanchez-Olea discloses the link interface comprises an optical input/output port (Fig. 1 Ref. 1106) for the purpose of providing a newer and faster interface.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the link interface comprises an optical input/output port as taught by Sanchez-Olea into the combined invention of Mote and Sharma for the advantages stated above.

11. Claims 26-31 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable Surti et al. (Surti) U.S. Patent No. 6,496,193 in view of Mote et al. (Mote) U.S. Patent No. 5,638,534.

As to claim 26, Surti discloses a computer system (Fig. 1), comprising: a central processing unit ("CPU") (Fig. 1 Ref. 11); a system controller (Fig. 1 Ref. 12) coupled to the CPU, the system controller having an input port and an output port (Fig. 1 Refs. 14-20); an input device (Fig. 1 Ref. 20) coupled to the CPU through the system controller; an output device (Fig. 1 Refs. 14-19) coupled to the CPU through the system controller; a storage device (Fig. 1 Refs. 14-19) coupled to the CPU through the system controller; a plurality of memory modules (Fig. 1 Ref. 14 and col. 3 lines 27-28).

However, Surti does not specifically disclose each of the memory modules comprising: a plurality of memory devices; and a memory hub, comprising: a link interface receiving memory requests for access to at least one of the memory devices; a memory device interface coupled to the memory devices, the memory device interface being operable to transmit memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests; a posted write buffer coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit the write memory requests to the memory device interface; and a read request path operable to transmit read memory requests from the link interface to the memory device interface and to transmit read data from the memory device

interface to the link interface; and a communications link coupled between the system controller and each of the memory modules for coupling memory requests and read data between the system controller and the memory modules in the respective memory modules.

Mote discloses each memory module, comprising: a plurality of memory devices (Fig. 1 Refs. 135); and a memory hub (Fig. 1 Ref. 130), comprising: a link interface receiving memory requests for access to at least one of the memory devices (Fig. 1 Ref. 130 and col. 2 lines 34-41); a memory device interface (Fig. 1 Ref. 130 to Ref. 135) coupled to the memory devices, the memory device interface being operable to transmit memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests (col. 2 lines 34-41); a posted write buffer (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit the write memory requests to the memory device interface (col. 1 lines 50- 59); and a read request path operable to transmit read memory requests from the link interface to the memory device interface and to transmit read data from the memory device interface to the link interface (Fig. 1 Ref. 130 to Ref. 135 and col. 2 lines 34-41) for the purpose of permitting continue with its next operation (col. 1 lines 50-59).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate each of the memory modules

comprising: a plurality of memory devices; and a memory hub, comprising: a link interface receiving memory requests for access to at least one of the memory devices; a memory device interface coupled to the memory devices, the memory device interface being operable to transmit memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests; a posted write buffer coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit the write memory requests to the memory device interface; and a read request path operable to transmit read memory requests from the link interface to the memory device interface and to transmit read data from the memory device interface to the link interface; and a communications link coupled between the system controller and each of the memory modules for coupling memory requests and read data between the system controller and the memory modules in the respective memory modules as taught by Mote into the system of Surti for the advantages stated above.

As to claim 27, Mote further discloses wherein the read request (col. 1 line 60 thru col. 2 line 8 & col. 9) path comprises a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to transmit memory requests to the memory device interface responsive to memory requests received from the link interface.

As to claim 28, Mote further discloses wherein the posted write buffer comprises coherency circuitry (col. 1 line 60 thru col. 2 line 8 & col. 10 lines 34-51 and comparison and pointer logic) that is operable to receive read memory requests from the link interface and is operable to determine if read data called for by the read request is stored in the posted write buffer and to generate a hit signal (Fig. 8 Ref. 230 and col. 10 lines 34-51, comparison and pointer logic reads on this limitation) responsive thereto, and wherein the memory sequencer is coupled to receive the hit signal from the posted write buffer and is operable to transmit memory requests to the memory device interface responsive to memory requests received from the link interface only in the absence of the hit signal (Fig. 8 Ref. 230 and col. 10 lines 34-51, comparison and pointer logic reads on this limitation).

As to claim 29, Mote further discloses wherein the posted write buffer (Fig. 8 Ref. 204 and col. 1 line 60 thru col. 2 line 8 & col. 9) is operable to transmit the write memory requests to the memory device interface only when neither the memory hub nor the memory devices are busy servicing read memory requests.

As to claim 30, Mote further discloses wherein the posted write buffer further comprises coherency circuitry (col. 1 line 60 thru col. 2 line 8 & col. 10 lines 34-51 and comparison and pointer logic) coupled to receive read memory requests from the link interface, the coherency circuitry being operable to determine from each read memory request whether the read memory request is directed to a memory address to which a

write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, the coherency circuitry being operable to transmit the read data responsive to the read memory request from the posted write buffer to the link interface in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface (col. 9 and col. 10 lines 34-51).

As to claim 31, Mote further discloses wherein the memory hub further comprises a multiplexer (col. 1 line 60 thru col. 2 line 8, data from posted write or DRAM reads on this limitation) having a first input port coupled to receive read data from the posted write buffer, a second input port coupled to receive read data from the memory device interface and an output port (Fig. 1 Ref. 192 D0-D31) coupled to the link interface to apply read data to the link interface, the multiplexer further having a control terminal (Fig. 8 outputs from Refs. 230 and 206 or Fig. 7 Ref. 186) coupled to the posted write buffer, the posted write buffer generating a control signal to cause the multiplexer to couple the output port to the first input port in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, and to generate a control signal (Fig. 8 outputs from Refs. 230 and 206 or Fig. 7 Ref. 186) to cause the multiplexer to couple the output port to the second input port in the event the read memory request is not directed to a memory address to which a write memory

request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

As to claim 38, Mote further discloses wherein the memory devices comprise dynamic random access memory devices (Fig. 1 Ref. 135).

12. Claims 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Surti et al. (Surti) U.S. Patent No. 6,496,193 in view of Mote et al. (Mote) U.S. Patent No. 5,638,534 and further in view of Shipp et al. (Shipp) U.S. Patent No. 5,796,413.

As to claim 32, Mote further discloses wherein the posted write buffer is operable to store posted write memory requests (Fig. 7 Ref. 184 and Col. 9. lines 1-27 and col. 1 lines 50-59). However, neither Surti nor Mote specifically discloses the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit the posted write memory requests to the memory device interface.

Shipp discloses the number of posted write memory requests accumulated exceeds a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65), and to thereafter transmit the posted write memory requests to the memory device interface for the purpose of preventing data overflow and underflow (col. 7 line 1).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit the

posted write memory requests to the memory device interface as taught by Shipp into the combined system of Surti and Mote for the advantages stated above.

As to claim 33, Surti, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to vary the predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) as a function of an operating parameter of the memory module.

As to claim 34, Surti, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to store posted write memory requests (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) until the posted write memory requests have been stored for more than a predetermined duration, and to thereafter transmit the posted write memory requests to the memory device interface.

As to claim 35, Surti, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to vary the predetermined duration (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) as a function of an operating parameter of the memory module.

As to claim 36, Surti, Mote and Shipp disclose the invention as claimed above. Shipp further discloses wherein the posted write buffer is operable to store posted write

memory requests as long as the number of posted write memory requests accumulated does not exceed a predetermined number (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65) and the posted write memory requests have not been stored for more than a predetermined duration (col. 6 line 64 thru col. 7 line 7 and col. 10 lines 50-65), and to transmit the posted write memory requests to the memory device interface if either the number of posted write memory requests accumulated exceeds the predetermined number or the posted write memory requests have been stored for more than the predetermined duration.

13. Claim 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Surti et al. (Surti) U.S. Patent No. 6,496,193 in view of Mote et al. (Mote) U.S. Patent No. 5,638,534 and further in view of Sanchez-Olea U.S. Patent Pub 2002/0178319.

As to claim 37, Surti and Mote disclose the invention as claimed above. However, neither Surti nor Mote specifically discloses the link interface comprises an optical input/output port.

Sanchez-Olea discloses the link interface comprises an optical input/output port (Fig. 1 Ref. 1106) for the purpose of providing a newer and faster interface.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the link interface comprises an optical input/output port as taught by Sanchez-Olea into the combined system of Surti and Mote for the advantages stated above.

As to claim 39, Surti, Mote, and Sanchez-Olea disclose the invention as claimed above.

Sanchez-Olea further discloses the communications link comprises an optical communications link (Fig. 1 Ref. 1106)

Response to Arguments

14. Applicant's arguments filed 12/12/05 have been fully considered but they are not persuasive.

Applicant's arguments filed on 12/12/05 have been fully considered but they are not persuasive.

In response to applicant's argument on page 18 that the prior arts do not disclose memory module has been fully considered but it is not persuasive.
Mote discloses a memory module (Fig. 1 Ref. 120, memory subsystem, since necessary memory command and controls (i.e. Fig. 2 Ref. 150-156) are from module 110 while memory subsystem is further controlled by Ref. 130 and also note that cache memory is also controlled by the module 110).

In response to applicant's argument on page 18 that the prior arts do not disclose a controller has been fully considered but it is not persuasive.
Sharma discloses a controller (Fig. 1 North Bridges).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Mote discloses each memory module for the purpose of permitting continue with its next operation (col. 1 lines 50-59). Therefore broadly written claims are disclosed by the references cited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
January 4, 2006